

EAST - [10085735.wsp:1]

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BRS:

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Active

L1: (67447) "455"/\$.ccls.

L2: (6168) L1 and (gain near3 control\$4)

L3: (1816) L2 and ("power amplifier" or PA)

L4: (9) L3 and (power near5 ratio near5 monitor\$3)

L5: (6) L4 and (variable near5 gain)

L6: (11750) (variable near3 gain) and (gain near3 control\$4)

L7: (2435) 6 and ("power amplifier" or PA)

L8: (6) 7 and "second order distortion"

L9: (2) 8 and (squa\$3 near3 circuit)

L10: (3) 8 and squa\$3

L11: (22) 7 and ("second order" near5 distortion)

L12: (1) 11 and BPF

L13: (12) 11 and "band pass filter"

L14: (11) 13 and multiplier

L15: (0) 14 and subtractor

L16: (11) 14 and subtract\$3

L17: (4) 14 and subtract\$3

L18: (4) 17 and wireless

L19: (4) 18 and antenna

L20: (4) 19 and transmitter

L21: (4) 20 and squa\$3

Failed

Saved

US 6803829 B2

Search

Find

Browse

Image

Open

Open

US:PGRUB:USPAT:EPD

Default operator: OR

20 and squa\$3

BRS form

IS&F form

Image

Text

HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current X	Ren	Inventor	IS
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6803829 B2	20041012	149	Integrated VCO having an improved tuning range over process and temper	331/34	257/E27.046		Duncan; Ralph et al.	<input checked="" type="checkbox"/>
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6759904 B2	20040706	123	Large gain range, high linearity, low noise MOS VGA	330/254	257/E27.046		Behzad; Arya R.	<input checked="" type="checkbox"/>
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6525609 B1	20030225	123	Large gain range, high linearity, low noise MOS VGA	330/254	257/E27.046		Behzad; Arya R.	<input checked="" type="checkbox"/>
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6426680 B1	20020730	152	System and method for narrow band PLL tuning	331/34	257/E27.046		Duncan; Ralph et al.	<input checked="" type="checkbox"/>

Drafts

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- ☑ L1: (67447) "455"/\$.ccls.
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- ☑ L6: (11750) (variable near3 gain) and (gain near3 control\$4)
- ☑ L7: (2435) 6 and ("power amplifier" or PA)
- ☑ L8: (6) 7 and "second order distortion"
- ☑ L9: (2) 8 and (squar\$3 near3 circuit)

Failed

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- ☑ S1: (1) ("6115406").PN.
- ☑ S2: (67447) "455"/\$.ccls.
- ☑ S3: (6168) S2 and (gain near3 control\$4)
- ☑ S4: (1816) S3 and ("power amplifier" or PA)
- ☑ S5: (9) S4 and (power near5 ratio near5 monitor\$3)
- ☑ S6: (6) S5 and (variable near5 gain)

Favorites

Tagged (1)

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(16) United States
 (17) Patent Application Publication
 Hayashihara
 (18) Pub. No.: US 2002/0123315 A1
 (19) Pub. Date: Sep. 5, 2002

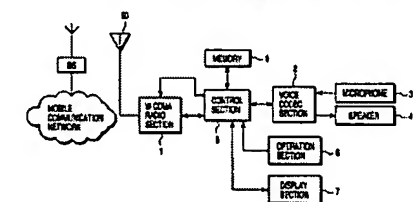
(20) RADIO COMMUNICATION TERMINAL AND
 GAIN CONTROL CIRCUIT FOR THE SAME
 (21) Inventor: Hayashihara, Mikio (JP)
 (22) ABSTRACT

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current X	Ref	Inventor	S
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20030186664 A1	20031002	16	Distortion reduction calibration	455/232.1	455/234.1; 455/236.1		Shah, Peter Jivan	<input checked="" type="checkbox"/>
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020123315 A1	20020905	9	Radio communication terminal and gain control circuit for the same	455/194.2	455/241.1		Hayashihara, Mikio	<input checked="" type="checkbox"/>

5 and (variable near5 gain)

NUM